Single-Carrier Phase-Disposition PWM Techniques for Multiple Interleaved Voltage-Source Converter Legs

Georgios Konstantinou, *Member, IEEE,* Gabriel J. Capella, Josep Pou, *Fellow, IEEE*, and Salvador Ceballos

***Abstract*—Interleaved converter legs are typically modulated with individual carriers per leg and phase-shifted PWM (PS-PWM) as it facilitates current balancing amongst the legs. Phase-disposition PWM (PD-PWM), despite the better harmonic performance, cannot be directly used due to the resulting current imbalance that may damage the converter. This paper addresses the current sharing issue and proposes a sorting algorithm implementation that enables single-carrier PD-PWM technique for interleaved two-level converter legs. An extension of the proposed algorithm through a switching state feedback loop, limiting the average switching frequency, is also developed. In both cases, the output current is of high quality and shared amongst the phase-legs, while the deviation between the phase-leg currents is well regulated. Simulation results demonstrate the general function of method for multiple interleaved legs as well as its current sharing capabilities for high-power applications. Experimental results from a low-power laboratory prototype validate the operation of the proposed approach.**

***Index Terms*—Interleaving, multilevel converters, multilevel waveforms, parallel legs, voltage source converters.**

I. Introduction

INTERLEAVING of power electronics converters or converter legs (Fig. 1) provides an alternative method of increasing the total current rating while avoiding the parallel connection of semiconductor devices, effectively increasing the power rating for a given voltage level [1]. Other advantages of interleaved converters include *i)* a modular solution with increased converter availability, *ii)* higher efficiency, *iii)* an equivalent multilevel waveform with reduced harmonic distortion [2]–[4] and *iv)* an economically optimal solution [5].

Typical applications of interleaved voltage source converters (VSCs) include uninterruptible power supplies (UPS) [1], [6], variable-speed motor drive systems (VSDs) and traction power supplies [7], [8]. Due to the increase in power from a single wind turbine over the last couple of years, interleaved converters are becoming more prevalent in wind-power applications [9]–[12] and they are also used in distributed power systems with parallel sources supplying common loads [5].

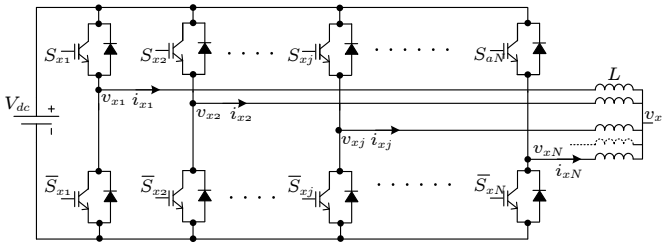

Fig. 1. Multiple interleaved two-level converter legs (phase x).

A number of control strategies have been proposed to enhance the operation of parallel converters with high-level communication including a low-bandwidth supervisory controller [13], distributed droop controllers [14], average controllers for power balancing among converters and a circular chain control with communication only between adjacent converters [15]. Ref. [16] proposed a modular current sharing control scheme for parallel converters.

The use of a centralized controller with common dc-voltage control and one or multiple current controllers is more common in high-power converters and applications with a common dc-voltage source, providing a better alternative to the parallel connection of semiconductors. Additionally, the larger amount of information available to the controllers provides greater flexibility and direct control of circulating currents that might be present [3]. A common controller further enables harmonic cancellation between interleaved converters by synchronizing their modulation.

Most of the earlier work on the topic handles interleaving through a phase-shift in the operation of the legs, generally implemented through phase-shifted pulse-width modulation [PS-PWM - Fig. 2(a)] [4], [11], [12], [17]–[20] or space-vector modulation (SVM) [2], [9], [21], [22]. This is required, as circulating current control based on external controllers requires individual references for each of the converter legs in order to adjust the conduction times to achieve the control targets. However, it is well established that the harmonic performance of both techniques is not optimal [23]. The application of selective harmonic elimination PWM (SHE-PWM) for interleaved converters was discussed in [3], with

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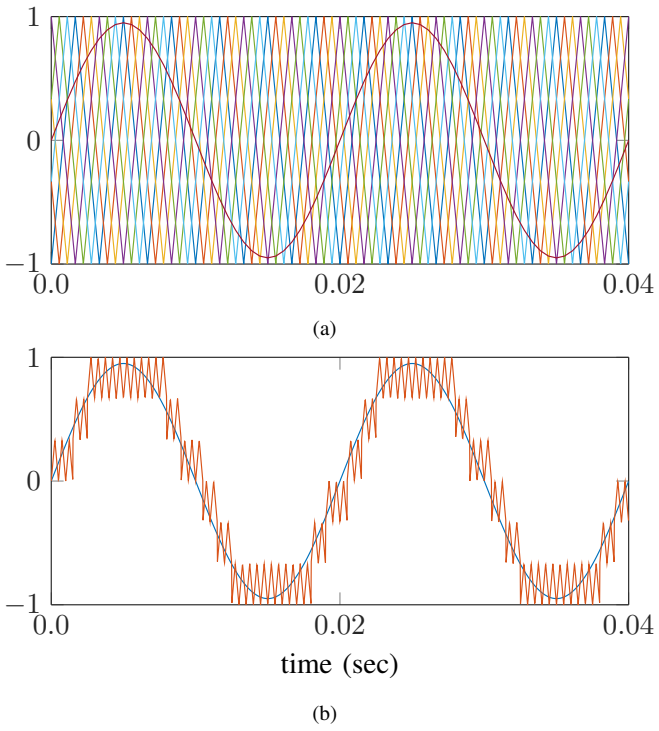


Fig. 2. Reference signal and carrier waveforms for multiple interleaved VSCs. (a) PS-PWM, and (b) PD-PWM.

the technique limited to low switching frequency operation.

Methods for enabling phase-disposition PWM [PD-PWM - Fig. 2(b)] in interleaved converter phase-legs have also been proposed [24]–[26] with the work of [24], [25] focusing on topologies with split-wound and three-phase coupled inductors. In [26], a state machine and a set of logical functions were proposed for determining the switching state of converter legs in an topology with two interleaved legs per-phase. Although suitable for a low number of converter legs, determining the switching logic between the increasing number of interleaved converter-legs becomes exponentially more complicated.

Driven by the application of sorting algorithms in modular multilevel converters (MMCs) and cascaded H-bridge converters (CHBs), this article proposes a current sorting algorithm that is easily scalable and can be applied for topologies with multiple interleaved converter legs. The use of a sorting algorithm provides a layer between the modulation and switching signal generation stages of a particular converter phase-leg, as typically occurs with PS-PWM, thus enabling interleaved converters to operate with PD-PWM and take advantage of the superior harmonic performance of the latter, compared to PS-PWM [23].

This paper is organised in the following manner. Section II reviews method of current control in interleaved convertters and Section III introduces basic concepts of interleaved converters. Section IV proposes the current sorting algorithm for parallel-connected legs. A variation of the proposed algorithm to eliminate redundant switching transitions in the phase-leg through a state feedback loop is also developed. Simulation results for multiple interleaved converter legs aimed at high-power applications are provided in Section V, and experimental results from a low-power laboratory prototype are provided in Section VI. Finally, the conclusions are summarized in Section VII.

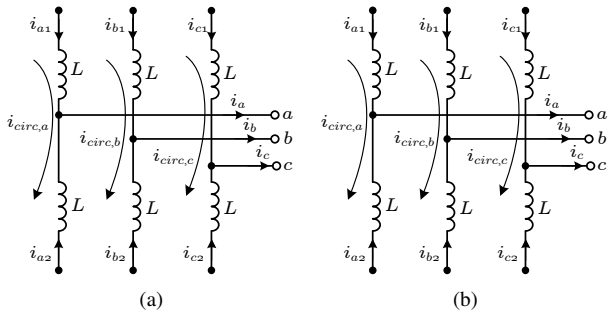


Fig. 3. Two legs connected in parallel in a three-phase converter. (a) Single and (b) coupled inductors for parallel connection of converter legs.

II. Current Control in Interleaved Converters

Interleaved operation through direct connection of parallel converter legs cannot be achieved because of short-circuits produced within the legs. Interleaving can be achieved with or without isolation between the ac and the dc-side of the converter. In the former case, transformers are included in the ac-side eliminating circulating currents between the converter legs and also the zero-sequence circulating current (ZSCC). However, the inclusion of transformers increases the size and weight of the overall system [16], also reducing its flexibility and modularity. In the latter case, inductors are used as passive elements to reduce the circulating current in the converter and also to average the voltage of each phase-leg. The use of a single inductor per leg (Fig. 3(a)) provides a simple, modular and expandable solution, however, practical limits in the maximum impedance [27] and the sub-optimal utilization of magnetic material are significant drawbacks. Coupled inductors (Fig. 3(b)) result in high differential mode impedance in the path between the interleaved converters, reducing both the voltage and output current ripples and providing a faster response to load current transients [28]. The concept that can be extended to multiple interleaved legs either with one common core or with multiple coupled inductors.

A flatness control for the parallel operation of voltage source inverters that considers the energy stored in the output filter inductors as the flat variables was proposed in [29]. A magnetic model to ensure current balance and to minimize the circulating current within high-power multiphase leg-coupled parallel-connected converters was presented in [30]. A low cost system for interleaved converter testing was developed in [31]. In [32] an analysis of the design of coupled inductors to be used in interleaved converters shows that PS-PWM (Fig. 2(a)) increases the losses within the coupling inductors of the system but provides higher quality currents. A trap filter for the output of interleaved converters was studied in [33] and as a result of several considerations on the design for the output filter, a combination of an LCL filter with an LC harmonic trap was proposed in [11]. A methodology for calculating the optimum angles of interleaved converters under PS-PWM with

unequal power sharing in order to minimize the grid current distortion was developed in [20] and a deadbeat controller for control of the circulating current was proposed in [34].

Ref. [19] presented a method to control the circulating currents for voltage source converters with magnetically coupled legs which introduced a variation of the duty ratio of each converter leg in order to minimize the circulating current under PS-PWM. An enhancement of PS-PWM that generates voltage waveforms with transitions between adjacent levels was proposed in [4]. The proposed method provides lower total harmonic distortion (THD) of the line to line voltage but the transition between the different waveform bands generates a small imbalance in the phase-leg currents that needs to be compensated. A simplified PWM technique with switching constraints, proposed in [35], aims at eliminating the loops that generate the circulating current.

A scheme to realize PD-PWM for parallel two-level VSCs is presented in [36]. Three phase-legs are connected in parallel by means of a coupled inductor and one carrier is sequentially allocated to the different legs in a round-robin manner; this helps reducing the circulating currents among the legs. However, an appropriate processing and scaling of the voltage reference signals has to be performed first in order to accommodate them in the carrier spanning region. Such adaptation is performed twice per carrier period, and every switching period is made up of three carrier periods.

In order to ensure that the positive and the negative volt-sec applied to the inductors are balanced every sampling time, some additional switching transitions are added each time a band change in the references is detected. Such band changes can be easily anticipated when the voltages references are steady signals but almost impossible to predict in a dynamic closed loop operation. Besides, the scheme does not include any method to ensure that the leg currents are equally shared and its modularity is very limited as it is linked to a determined magnetic structure.

III. Analysis of Interleaved Phase-Legs

One phase of the multiphase system (Fig. 1) can be described as:

$$\mathbf{V_x} = \mathbf{L}\frac{d}{dt}\mathbf{I_x} + \mathbf{V_{x0}} \tag{1}$$

where $x \in \{a, b, c\}$ denotes the phase and $j \in \{1, \ldots, N\}$ denotes each of the N interleaved converters and

$$\mathbf{V_x} = \begin{bmatrix} v_{x1} \\ v_{x2} \\ \vdots \\ v_x \end{bmatrix}, \mathbf{I_x} = \begin{bmatrix} i_{x1} \\ i_{x2} \\ \vdots \\ i_x \end{bmatrix}, \mathbf{V_{x0}} = \begin{bmatrix} v_{x0} \\ v_{x0} \\ \vdots \\ v_{x0} \end{bmatrix}, \tag{2}$$

while $\mathbf{L}$ depends on the coupling amongst the inductors in the legs. Assuming that uncoupled inductors are used per phase-leg, then

$$\mathbf{L} = \begin{bmatrix} L & 0 & \cdots & 0 \\ 0 & L & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & L \end{bmatrix}. \tag{3}$$

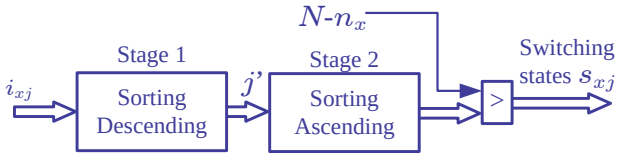


Fig. 4. Current sorting algorithm for parallel-connected legs.

The current from each phase is the sum of the currents from each of the legs as is

$$i_x = \sum_{j=1}^{N} i_{xj}, \tag{4}$$

while the equivalent Thevenin voltage of one phase $v_{x,com}$ is given by

$$v_{x,com} = \frac{1}{N}\sum_{j=1}^{N} v_{xj}. \tag{5}$$

From (5), it can be inferred that the equivalent voltage is a multilevel waveform with $N+1$ voltage levels based on which PD-PWM techniques can be developed.

IV. Current Sorting Algorithm

A. Direct Implementation

Sorting algorithms have received increased attention over the last decades, predominantly in MMCs as well as CHBs [37]–[39] converters in order to balance the sub-module (SM) or cell capacitor voltages. The proposed sorting algorithm for interleaved converter uses the measured current through each of the converter legs (i_{xj}) in order to determine which legs should generate positive and negative voltage in order to derive the required voltage level in the converter output.

The proposed implementation is shown in Fig. 4. Each of the legs has only two possible switching states, connected to either the positive or the negative dc-link. These two states have a predetermined effect on the current through the phase-leg. The algorithm determines the state of each phase-leg based on the instantaneous current through each one of them.

The sampled values of the currents through each of the legs (i_{xj}) are sorted from high to low (descending order) with the index of each element generating a sorted list of elements (j'). The second stage sorts the elements of j' in an ascending manner with the algorithm again using the indices of the sorting. This second sorting stage similarly to the case of the SM capacitor voltage balancing, generates a list with the priority order of each of the legs. The modulation stage, as shown in Fig. 2(b), generates the required number of legs (n_x). Through a simple comparison of n_x with the activation order, the switching state of each phase-leg is generated. Legs whose priority order is below or equal to n_x are connected to the positive dc-link while the rest are connected to the negative one.

The implementation of Fig. 4 ensures that the phase-legs will be connected in such a manner that the higher currents tend to decrease and the lower currents tend to increase. This means that each phase-leg will share the load current equally

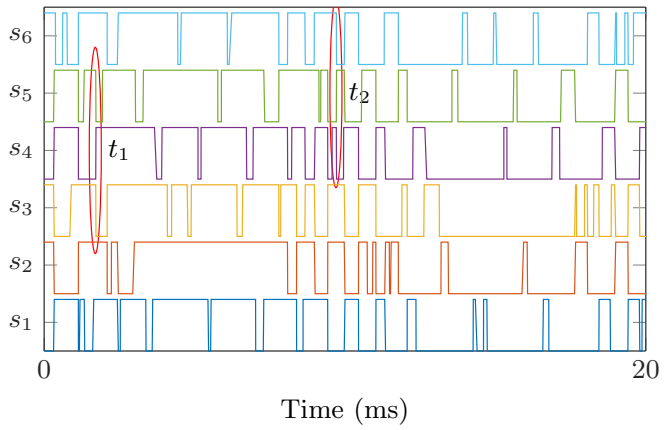


Fig. 5. Switching states of parallel-connected converter legs under the current sorting algorithm of Fig. 4.

while the circulating current amongst all legs will be kept to a minimum.

An unintended consequence of the method is that, as it continuously exchanges the legs in order to maintain the sharing of the load current i_x, multiple transitions can happen at the same time. For instance, when increasing one voltage level, two legs may commute to the positive dc-rail and one leg to the negative dc-rail. This leads to excessive transitions and to an increase in the switching frequency that is not reflected in the quality of the output waveforms. As an example to illustrate this behavior, Fig. 5 shows the switching states of a generic converter with a random number of parallel-connected legs. Multiple transitions at certain time instants (e.g. $t_1, t_2, \ldots$) can be observed. The next section will develop a feedback loop to minimise the number of transitions and to limit the switching frequency of each phase-leg.

B. Extended Implementation

In order to address the increase of the switching frequency from the implementation of the current balancing algorithm of Fig. 4, a feedback loop of the switching states (s_{xj}) of each phase-leg is proposed. The feedback loop, by supplying the current state of the legs, provides a way to limit the number of legs that can change their state to the number of level changes in the output voltage n_x. This means that no leg will switch unless there has to be a change in the level of the output voltage, or that only one leg will change its state if there has to be a change of one level in the output voltage, for instance.

The modified algorithm, shown in Fig. 6, changes the value of the phase-leg current used in the sorting stages depending on the switching state, by subtracting the value of $s_{jx} \cdot \Delta I$ so that the virtual phase-leg currents are given by:

$$i'_{xj} = i_{xj} - s_{xj}\Delta I, \tag{6}$$

The value of ΔI should be chosen in such a way that provides sufficient separation between the virtual phase-leg currents in the sorting stages. A value close to the nominal current of the converter is recommended, but any value sufficiently large to guarantee proper operation can be chosen at this stage.

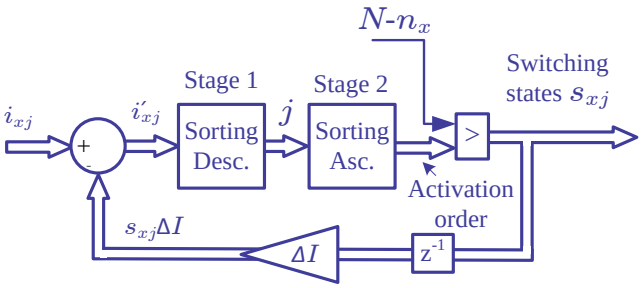


Fig. 6. Modified current sorting algorithm with the inclusion of a state feedback loop for reduction of the phase-leg switching frequency.

TABLE I
PARAMETERS OF SIMULATION AND EXPERIMENTAL PROTOTYPE

Parameter	Simulation	Experiment
Number of legs, n	6	4
dc-link voltage, V_{dc}	1000 V	60 V
dc-link capacitor, C_{dc}	3 mF	3 mF
Inductors, L	800 μH	6 mH
Carrier frequency f_{car}	3 kHz	5 kHz
Output frequency f	50 Hz	50 Hz
ΔI	2500 A	10 A

V. Simulation Results

To verify the proposed current sorting algorithm for multiple parallel-connected converter legs, a simulation of a 2 MW three-phase system with six ($n = 6$) legs connected in parallel is implemented in Simulink/PLECS. Table I summarizes the main system parameters while Fig. 7 shows the implementation of one phase of the circuit and its control. The converter is modulated with a single reference signal using PD-PWM as shown in Fig. 2(b). The purpose of the simulation results is to demonstrate the operation of the method with relatively low switching frequency, closely matching a practical application of interleaved converters.

The set of simulation results uses both implementations of the proposed current sorting algorithm with a transition between the two occurring at 0.1 sec. In both cases, the multilevel equivalent voltage at the output of the converter generates high quality load voltages and currents, as shown in Fig. 8. The total current through each phase (i_x) of the converter is shared amongst the phase-legs, as shown in Fig. 9(a). However, the balancing is driven by the mechanism described in the previous section. Unlike the current balancing of PS-PWM modulated legs, the fundamental component and higher order harmonics over consecutive periods will differ between different legs. This is illustrated in the harmonic spectra of the phase-leg currents (Fig. 9(b)) which correspond to a fundamental period randomly chosen among the ones in Fig. 9(a) after enabling the state feedback loop.

An additional consequence of the sorting algorithm and the variation of currents and switching patterns for the converter legs over multiple periods is that the losses within one fundamental period are not equally distributed amongst

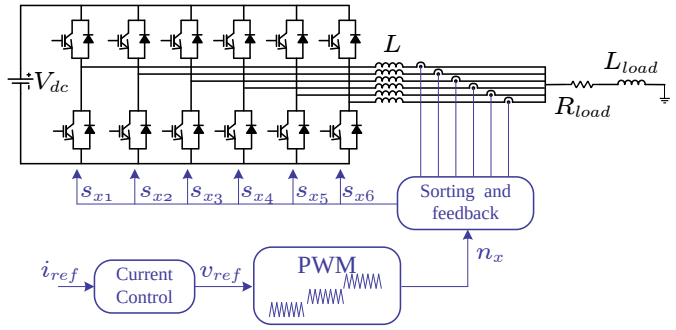
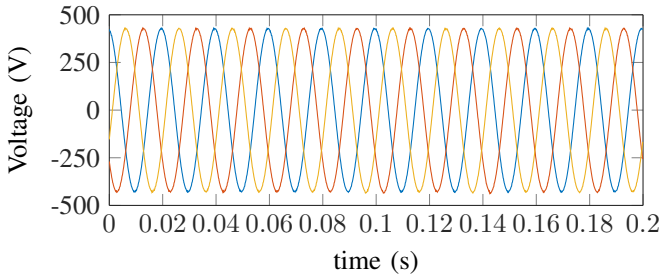
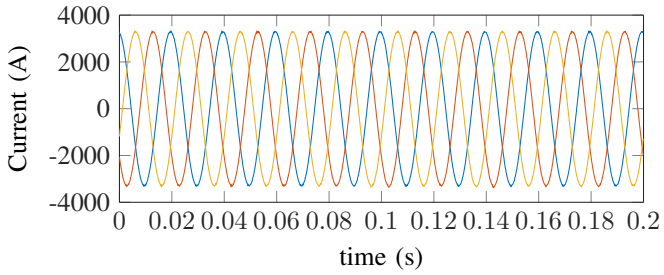


Fig. 7. Control Scheme of the proposed method applied to one of the phases.



(a)

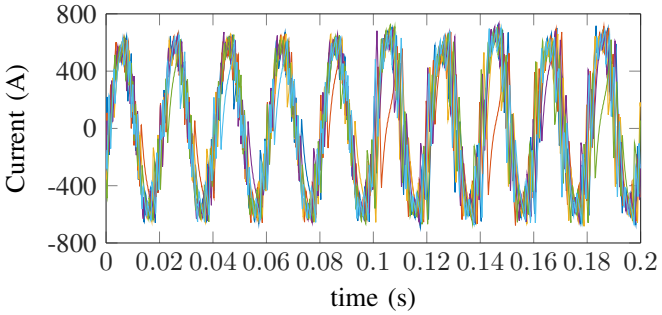


(b)

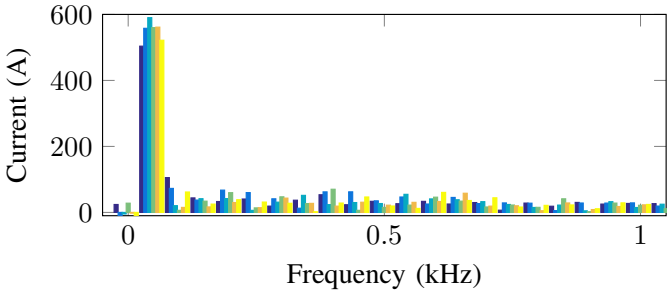
Fig. 8. Output waveforms. (a) Three-phase load voltages and (b) three-phase load currents.

the converter legs and balance over multiple periods, as are the switching transitions. This is demonstrated in Fig. 10, where the switching and conduction losses for each leg, locally averaged over a 20 ms window, and normalized to the average losses of a converter (the total converter losses divided by the number of converter legs), are shown in Fig. 10 for a total duration of 0.4 s. The state feedback loop is enabled at 0.2 sec.

Although it can be seen that the total losses of the converter for a given implementation remain constant, variations of up to 40% from the average switching losses and up to 30% from the average conduction losses can be observed within one fundamental period between the converter-legs. The instantaneous losses are irregularly scattered among the legs of the converter depending on the number of interleaved converter legs, the switching frequency and the leg current allocation. At higher frequencies than those used in our simulation studies, the instantaneous deviation of one converter leg from the average would be significantly smaller. Furthermore, it can also be noticed that such deviations increase when the state feedback is activated, on account of the switching limitations

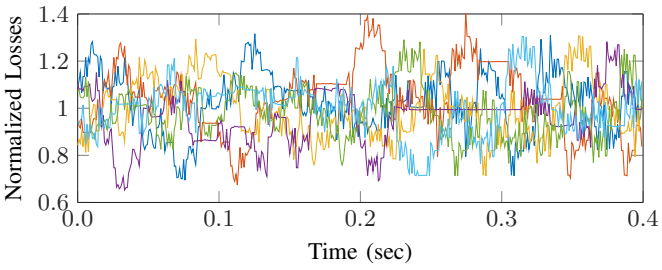


(a)

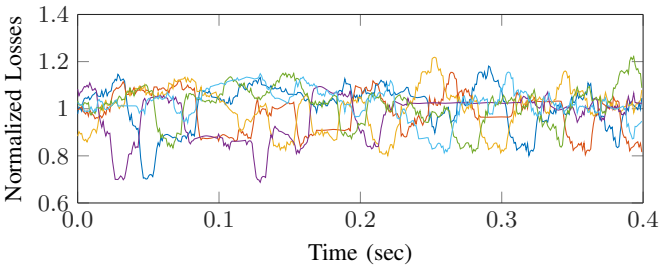


(b)

Fig. 9. (a) Measured phase-leg currents of phase a showing the current sharing among converter legs. State feedback loop enabled at 0.1 s. (b) Harmonic spectra of the phase-leg currents when the state feedback is enabled.



(a)



(b)

Fig. 10. Normalized distribution of losses to the converter legs, (a) Switching Losses and (b) Conduction Losses. State feedback loop is enabled at 0.3 sec.

imposed.

The impact of the feedback loop in the currents seen by the sorting stage, which leads to the elimination of additional transitions and reduction in the switching frequency of each converter leg, is shown in Fig. 11. The figure shows the virtual value of the sampled currents of phase a (i'_{aj}), which is used solely within the sorting algorithm stages of the proposed implementation. At $t = 0.1$s, the feedback loop is enabled

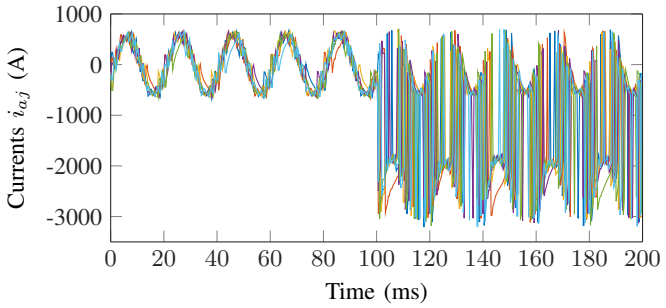


Fig. 11. Virtual phase-leg currents used in the sorting stages of the proposed method, i'_{aj} with the state feedback enabled at 0.1 sec.

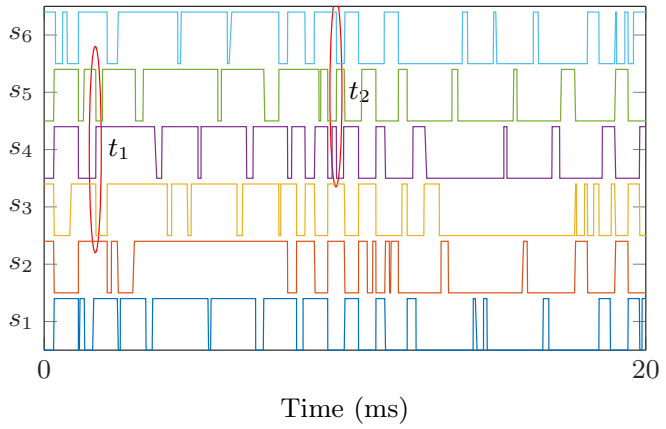


Fig. 12. Detail of the switching signals of the parallel-connected converter legs. State feedback loop enabled at 0.1 sec.

and the current of the legs that generate positive voltages is negatively offset by ΔI, while an increase in the actual phase-leg current ripple (Fig. 9(a)), due to the decrease in the switching frequency of the converter.

Fig. 12 shows the gating signals for the six converter-legs of phase a for one period before and after enabling the feedback loop. It can be seen that when the feedback loop is enabled only one transition occurs per each level change, reducing the switching frequency of each leg to f_{car}/N (500 Hz in this case) while maintaining the effective switching frequency of the output waveforms to f_{car}.

Through implementation of the current sorting algorithm, the interleaved converter legs can operate under PD-PWM with a single reference signal and carrier waveforms shown Fig. 2(b). A comparison between the implemented PD-PWM and a typical PS-PWM, as commonly used in the literature (see [12], [19], [40]) in terms of %THD and %WTHD of the line-to-line voltage considering the first 2000 harmonics, is shown in Figs. 13(a) and (b), respectively. The figures demonstrate that through the application of PD-PWM, the %THD is reduced by approximately 30% and the %WTHD is reduced by approximately 50% in the most commonly used operating regions of a converter ($M \in [0.5, 1]$). The superior performance of the method can also be confirmed by time-domain based analysis, as in [41].

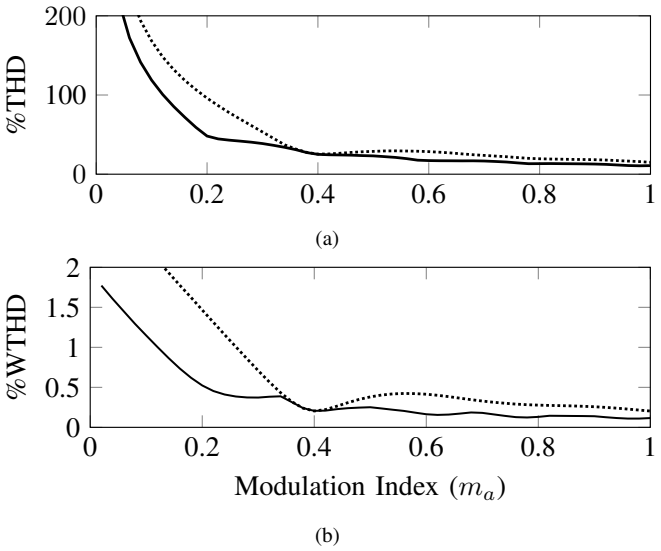


Fig. 13. Comparison between line-to-line voltages of PD-PWM (solid line) and PS-PWM (dotted line) with $N = 6$ parallel-connected legs. (a) %THD and (b) %WTHD.

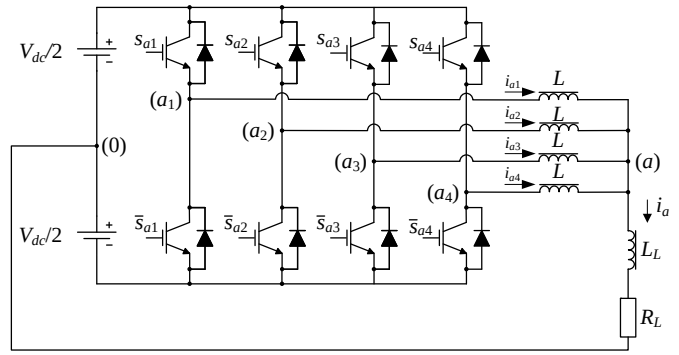
VI. Experimental Results

Experimental validation of the proposed controllers of Figs. 4 and 6 is performed on a setup consisting of a single-phase, two-level converter with four-legs in parallel as shown in Fig. 14. The parameters of the prototype converter and the load are given in Table I. The control, modulation and protection algorithms are implemented in a dSPACE ds1103 platform. The switching frequency (f_s=5 kHz) used in the experimental setup is a result of the relatively low inductances in each converter leg compared to the simulation case as well as the lower number of legs connected in parallel.

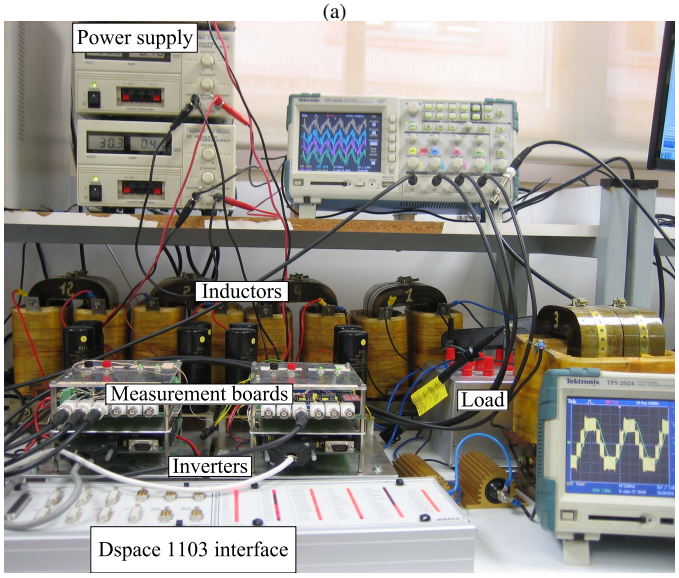
The first set of experimental results demonstrates the output of the converter as well as the current sharing capacity the proposed control structure, both with and without the state feedback loop. The voltage output of the four interleaved converter-legs and the voltage applied across the load is in both cases a five-level waveform, following (5). The total current is shared amongst the four converter-legs while the inclusion of the state feedback loop in the controller (Fig. 15(b)) leads to a reduction in the switching frequency of the converter-legs at the cost of a less tight regulation of the current among the three converter legs.

The impact of the state feedback loop on the apparent switching frequency can be better observed from the results in Fig. 16, where the cumulative count of switching transitions in the four converter legs are shown for a time frame of 0.1 s, with and without the state feedback loop. It is evident that inclusion of the feedback loop results in a substantial decrease of the switching frequency of each leg, as the simultaneous multiple transitions between legs are effectively restricted. In both cases, the apparent frequency of the output voltage waveform remains the same (at 5 kHz) and so are both the output current i_a and %THD of v_a.

The transient performance of the proposed method under changes in the converter operating point is illustrated with a step change in m_a from 0.3 to 0.9, shown in Fig. 17

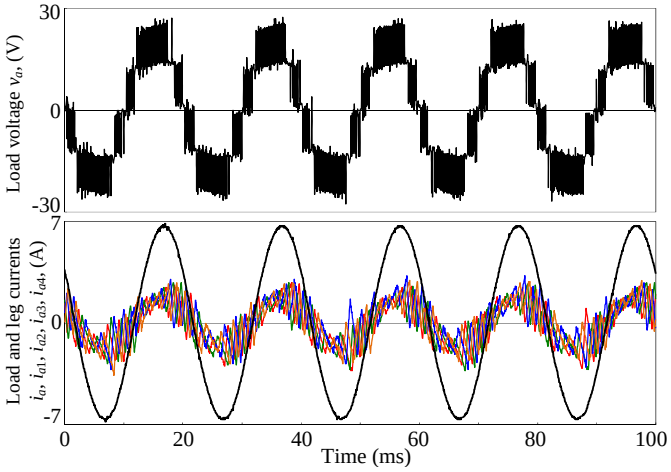


(a)

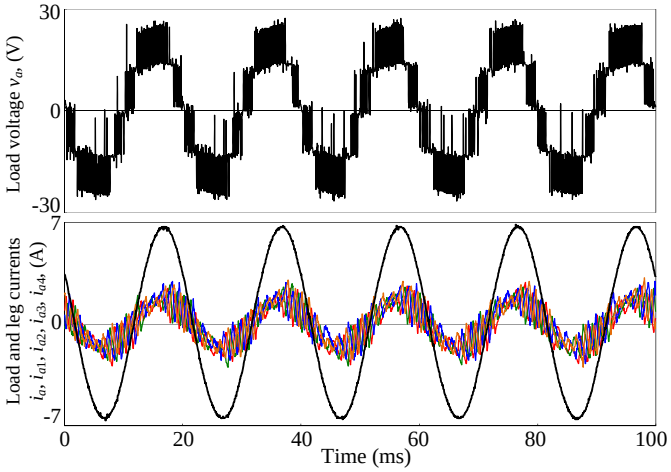


(b)

Fig. 14. Laboratory setup with four interleaved converter legs., (a) Schematic diagram for four interleaved phase-legs and (b) photo of the setup.



(a)



(b)

Fig. 15. Experimental results of four interleaved converter-legs, (a) without state feedback (Fig. 4) and, (b) with state feedback (Fig. 6)

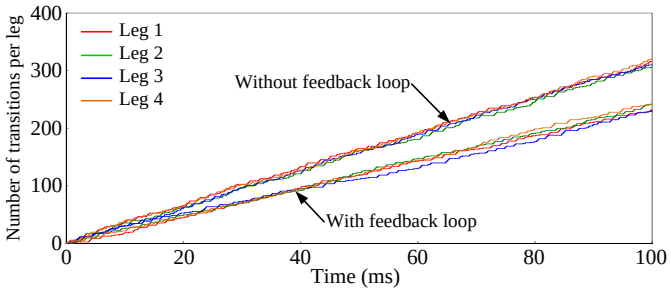


Fig. 16. Number of switching transitions in the three converter-legs without and with the state feedback loop.

with the state feedback loop enabled. At $t = 50$ ms, the modulation index changes resulting in a change in the voltage waveform from three-level to five-level. The detail of Fig. 17 shows that at any given instant, only one of the converter legs switches, demonstrating the function of the feedback loop in restricting the switching of the converter. The quality of the output current, due to interleaving, is high under both operating conditions. Current sharing among the converter legs is achieved, in alignment with the results of Fig. 15(b). The switching transitions are distributed equally among the four converter legs, as also seen in the switching patterns of Fig. 17.

VII. Conclusion

Interleaved two-level converters typically operate with PS-PWM where each phase-leg is associated with one carrier signal, providing current balancing, unlike PD-PWM which leads to unregulated phase-leg currents. This paper develops a current sorting algorithm that decouples the PWM patterns from the association to any specific phase-leg and thus enables the use of single-carrier PD-PWM techniques in converter-legs connected in parallel. The separation of modulation and switching signal generation stages means that other modulation techniques can also be implemented. In order to eliminate unnecessary transitions in the converter legs, a state feedback loop is also introduced in the proposed algorithm. Simulation and experimental results demonstrate the operation of the proposed method, the current sharing capability among the converter legs and the effective reduction in switching frequency due to the state feedback loop, while transition and loss equalization occurs at longer time intervals.

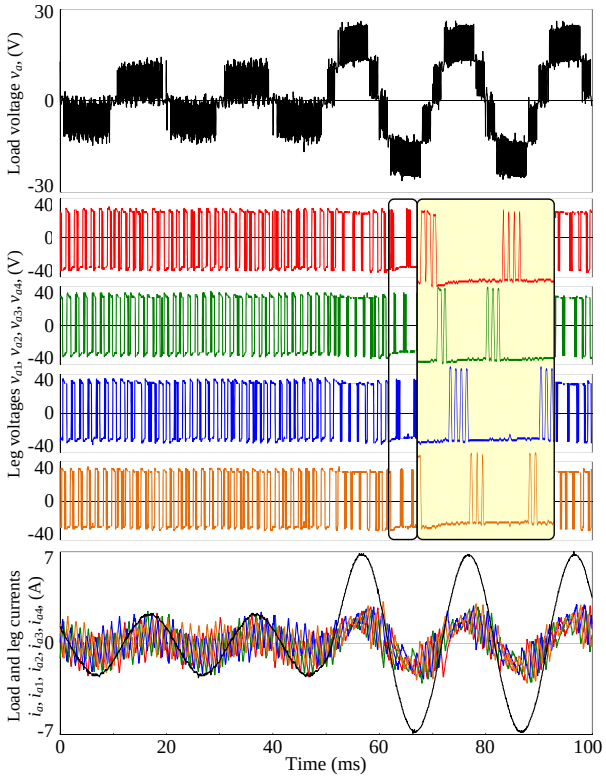


Fig. 17. Transition from $m_a = 0.3$ to $m_a = 0.9$. From top to bottom: Load voltage, four individual leg voltages and, load and leg currents, including a detail of the switching patterns for $m_a = 0.9$.

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